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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/672,180
Filing Date: September 26, 2003
Appellant(s): CHENG ET AL.

Christopher J. Reckamp
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2 September 2008 appealing from the Office action mailed 30 October 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,742,139	FORSMAN ET AL.	5-2004
2002/0093505	HILL ET AL.	7-2002

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

A. Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5-7, 10, 11, 24, 25, 26, 28-30, and 32-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,742,139 to Forsman et al. (hereinafter Forsman).

With respect to claim 1, Forsman discloses a circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor (column 4, lines 25-27 – host processor monitors service processor) by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor (column 4, lines 9-12 and lines 25-45 – heartbeat signal and status/control register indicate whether service processor functions correctly); and

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 2, Forsman discloses wherein an operating system executes on the processor (column 4, lines 4-5).

With respect to claim 5, Forsman discloses:

a halt communications module operative to halt command communications with the co-processor, in response to detecting a hang in the co-processor (column 5, lines 10-22 – warning sent to service processor followed by wait period);

a reset check module operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor (column 5, lines 28-33); and

a restart communications module operative to restart command communications with the co-processor, in response to detecting that the co-processor has been successfully reset (column 5, lines 33-35).

With respect to claim 6, Forsman discloses a method of monitoring and resetting a co-processor comprising:

detecting a hang in the co-processor (column 4, lines 25-27 – host processor monitors service processor) by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor (column 4, lines 9-12 and lines 25-45 – heartbeat signal and status/control register indicate whether service processor functions correctly); and;

selectively resetting the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 7, Forsman discloses wherein an operating system executes on the processor (column 4, lines 4-5).

With respect to claim 10, Forsman discloses:

halting command communications with the co-processor, in response to detecting a hang in the co-processor (column 5, lines 10-22 – warning sent to service processor followed by wait period);

detecting if the co-processor has been successfully reset, in response to the resetting of the co-processor(column 5, lines 28-33); and

restarting command communications with the co-processor, in response to detecting that the co-processor has been successfully reset (column 5, lines 33-35).

With respect to claim 11, Forsman discloses a circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor (column 4 lines 25-27 – host processor monitors service processor);

a halt communications module operative to halt executable instruction communications with the co-processor, in response to detecting a hang in the co-processor (column 5, lines 10-22 – warning sent to service processor followed by wait period);

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35);

a reset check module operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor (column 5, lines 28-33); and

a restart communications module operative to restart executable instruction communications with the co-processor, in response to detecting that the co-processor has been successfully reset (column 5, lines 33-35).

With respect to claim 24, Forsman discloses a memory containing instructions executable on a processor that causes the processor to:

detect a hang in a co-processor by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor (column 4, lines 9-12 and lines 25-45 – heartbeat signal and status/control register indicate whether service processor functions correctly); and

selectively reset the co-processor without resetting the processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 25, Forsman discloses instructions that causes the processor to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor (column 5, lines 28-33).

With respect to claim 26, Forsman discloses a circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor (column 4, lines 25-27 – host processor monitors service processor) by detecting a discrepancy between a current state of the co-processor and data in one or more storage elements associated with the co-processor, wherein the data in the one or more storage elements represents a current activity of the co-processor (column 4, lines 9-12 and lines 25-45 –

heartbeat signal and status/control register indicate whether service processor functions correctly); and

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 28, Forsman discloses wherein the hang detector module is operative to determine if the data in the one or more storage elements reflects processing of instructions by the co-processor (column 4, lines 36-45).

With respect to claim 29, Forsman discloses wherein the current state of the co-processor is represented by data stored in the one or more storage elements associated with the co-processor (column 4, lines 36-45).

With respect to claim 30, Forsman discloses a method of monitoring and resetting a co-processor comprising:

detecting a hang in the co-processor (column 4, lines 25-27 – host processor monitors service processor) by detecting a discrepancy between a current state of the co-processor and data in one or more storage elements associated with the co-processor, wherein the data in the one or more storage elements represents a current activity of the co-processor (column 4, lines 9-12 and lines 25-45 – heartbeat signal and status/control register indicate whether service processor functions correctly); and

selectively resetting the co-processor without resetting a processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 32, Forsman discloses determining if the data in the one or more storage elements reflects processing of instructions by the co-processor (column 4, lines 36-45).

With respect to claim 33, Forsman discloses wherein the current state of the co-processor is represented by data stored in the one or more storage elements associated with the co-processor (column 4, lines 36-45).

With respect to claim 34, Forsman discloses a memory containing instructions executable on a processor that causes the processor to:

detect a hang in a co-processor (column 4, lines 25-27 – host processor monitors service processor) by detecting a discrepancy between a current state of the co-processor and data in one or more storage elements associated with the co-processor, wherein the data in the one or more storage elements represents a current activity of the co-processor (column 4, lines 9-12 and lines 25-45 – heartbeat signal and status/control register indicate whether service processor functions correctly); and

selectively reset the co-processor without resetting the processor, in response to detecting a hang in the co-processor (column 4, lines 27-35).

With respect to claim 35, Forsman discloses wherein the discrepancy is detected by comparing data representing a current state of the co-processor (column 4, lines 36-50 – status/control register) with data representing a current activity of the co-processor (column 4, lines 25-35 – heartbeat signal).

B. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forsman in view of U.S. Patent App. No. 2002/0093505 to Hill et al. (hereinafter Hill).

With respect to claim 12, Forsman does not disclose expressly wherein the processor is a host processor and the co-processor is a graphics processor.

Hill discloses a system in which a graphics processor works with the main CPU to execute graphic-intensive software (paragraph 21 - graphics processor referred to as "graphic accelerator"). Hill's system prevents the entire computing system from crashing due to a failure specific to the graphics accelerator, by performing a series of

tests (paragraph 23, lines 1-16). If the graphics accelerator does not perform adequately, the software graphics processor will take over instead of crashing the system (paragraph 34, last 4 lines, paragraph 35). Hill discloses that he intends to improve situations where a reset due to a graphics processor crash is unacceptable (paragraph 19, last 8 lines). Forsman also wishes to recover a system of multiple processors without performing a full system reset (Forsman - column 1, lines 25-29). Using a graphics processor in place of a service processor in Forsman's system would prevent system crashes due to graphics accelerators as well as the service processor, preventing crashes due to incompatible video accelerators or other faults. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the graphics accelerator monitoring system of Hill into the processor reset system of Forsman, providing additional protection against hardware failure.

With respect to claim 13, Forsman discloses wherein the hang detector module detects the hang in the graphics processor by detecting a discrepancy between a current state of the graphics processor and a current activity of the graphics processor (column 4, lines 9-12 and lines 25-45 – heartbeat signal and status/control register indicate whether service processor functions correctly).

(10) Response to Argument

A. Claims 2, 6-7, 12-13, and 24 stand or fall together with independent claim 1

With regard to claim 1, appellant has indicated disagreement that Forsman teaches each and every limitation claimed. In particular, appellant argues that Forsman does not disclose detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor. Instead, appellant summarizes Forsman as follows.

> "Forsman is limited to a system and method that (1) resets a service processor when a host processor fails to detect a heartbeat signal from the service processor, or (2) resets a service processor when (a) a host processor fails to detect a heartbeat signal from the service processor, and (b) the host processor determines that conditions do not exist that preempt the host processor from resetting the service processor. In the first instance, Forsman fails to detect any sort of discrepancy between two things such as a current state and a current activity of a co-processor. In the second instance, Forsman resets the service processor only after determining a consistent condition between the lack of heartbeat signals and a lack of preempting conditions."
> (Appeal Brief, page 14-15)

The examiner respectfully disagrees with this interpretation of Forsman. Firstly, Forsman clearly teaches only instance (2) as described by appellant - see column 4, lines 25-50 and figure 3. In this portion, Forsman describes (a) a heartbeat signal transmitted from service processor to host processor, and (b) a status/control register

located in hardware logic of the service processor (both also illustrated in figure 2). A heartbeat signal can either be received by the host processor, or not received by the host processor (column 4, lines 10-12 and lines 35-37). Additionally, the status/control register can indicate a special status (column 4, lines 40-45), or inherently, a normal status if no special status is indicated. In order to detect a hang of the service processor, two events must occur – a heartbeat signal is not received, and the status/control register must indicate a normal status of the service processor.

The examiner submits that this situation is equivalent to a discrepancy between a current state of the co-processor and a current activity of the co-processor, as recited in the claims. Since the heartbeat signal (current activity) is not received, but the status/control register (current state) indicates that it should be received because the service processor is in a normal state, a discrepancy exists, and the service processor is considered to be in a hang condition. Considering another situation, in which a heartbeat signal is not received and the status/control register indicates a special status, no discrepancy exists. Because the status/control register indicates a special status, it is clear to the host processor that the service processor is not in a hang condition, and the lack of heartbeat signal is ignored (see column 5, lines 7-10).

Appellant alleges that the situation in which the heartbeat signal is not received and the status/control register indicates a normal status describes a consistent condition and not a discrepancy, however, the examiner is unable to follow this line of reasoning. As determined above, this situation represents conflicting states, in which a heartbeat signal should be received (because the service processor is in a normal state), but is

not received at the host processor. The examiner believes that this description reasonably falls under the definition of "discrepancy," as would be known to one of ordinary skill in the art. Since appellant has not defined or used the term "discrepancy" to rebut its plain and ordinary meaning, it is taken as such.

For at least this line of reasoning, the examiner determines that Forsman teaches detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor, as recited in claim 1.

B. Claims 28, 30, 32, and 34 stand or fall together with independent claim 26

Regarding claim 26, appellant uses an identical argument as applied to claim 1. Namely, that Forsman discloses determining a consistency, and not a discrepancy, between a lack of heartbeat signal and lack of preempting conditions (Appeal Brief, page 19-20). Again, the examiner is unable to follow this line of reasoning. Appellant states that the lack of status exceptions are indications that the service processor is in a hang condition (Appeal Brief, page 20), however, this is simply not true. When the service processor is in a normal status, and therefore shows lack of status exceptions, this simply indicates the service processor is in a normal, or non-special, state. On the other hand, the combination of both a lack of heartbeat signals and an indication of normal status is necessary for indication of a hang condition. This situation, as described above, indicates a hang condition because of a discrepancy between the heartbeat and status/control register. The status/control register indicates a lack of

status exceptions, and therefore a heartbeat should be received. However, a heartbeat signal is not received. This results in a hang condition whereupon the service processor is reset. For at least these reasons, the examiner submits Forsman discloses each limitation as recited in claim 26.

C. Claims 29 and 33 stand or fall together with claim 35

Claim 35 recites wherein the discrepancy is detected by comparing data representing a current state of the co-processor with data representing a current activity of the co-processor. Appellant argues that Forsman does not teach this limitation. However, as discussed previously in relation to claims 1 and 26, Forsman teaches receiving two articles of data – data relating to the heartbeat signal and data relating to the service processor status as retrieved from the status/control register. While appellant's Appeal Brief insists the lack of a heartbeat signal is equivalent to lack of data (page 21), the examiner disagrees. Given the lack of a heartbeat signal, the host processor retains data signifying that there is a lack of a heartbeat signal. The host processor also retrieves data concerning the state of the service processor from the status/control register. Through comparison of the two pieces of data (i.e. both must contain certain values), the host processor determines a hang condition in the service processor, and proceeds to reset the service processor.

Appellant's specification does not define "comparing" beyond its plain and ordinary meaning, and claim 35 does not further limit the process of comparing by, for example, reciting how data is compared, when data is compared, etc. Furthermore, the

process as described in the appellant's specification is similar to Forsman. According to paragraph 36 of the specification, there are two steps in determining a hang condition. First a busy flag is checked, or, in other words, a current state of the co-processor is determined. Then, register activity (recited as current activity in the claims) is monitored and values are compared to determine if the co-processor is reading and writing to the registers. Thus, in order to determine a hang condition there must exist a combination of the busy flag being set and no register activity (as explicitly recited in allowed claim 14). Similarly, in Forsman, to determine a hang condition there must be a lack of heartbeat signal and a normal state of the service processor. Thus, both appellant's invention and Forsman retrieve and analyze two pieces of data to determine a hang condition in a co-processor. Beyond this embodiment, the specification, as well as claim 35, does not further limit the subject matter. Claim 35, in fact, simply recites comparing data representing a current state and data representing a current activity, which the examiner believes is reasonably taught by Forsman.

For at least this line of reasoning, the examiner has determined that Forsman discloses each limitation as recited in claim 35.

D. Claims 5 and 10 stand or fall together with independent claim 11

With regard to claim 11, appellant argues that Forsman does not disclose a halt communications module operative to halt executable instruction communications with the co-processor, in response to detecting a hang in the co-processor. More particularly, Forsman teaches a timeout period, without mention of a halt

communications module, which is not the same as the claimed halt communications module for halting executable instruction communications with the co-processor.

The examiner respectfully disagrees with this argument. Analyzing the language of the claim against Forsman, the host processor of Forsman is clearly "a circuit" (figure 1, items 101-104 and column 2, lines 11-18) for monitoring and resetting a co-processor (column 3, lines 37-40). Furthermore, a "module" can describe either hardware or software, which the claims do not specify. Regardless, the host processor of Forsman is inherently controlled by either software instructions or a hardware circuit that cause it to wait for an acknowledgement from the service processor (see column 5, lines 10-22 and figure 3, steps 304-306).

Appellant additionally appears to assume that Forsman does not state that communication between the host processor and service processor has been halted. However, Forsman clearly defines the process in figure 3. According to step 304, the host processor sends a warning to the service processor that a hard reset is about to occur. Then, in step 306, the host processor determines whether an acknowledgement is received or a timeout has occurred. Further explained in column 5, lines 19-22, "the timeout period is a predefined interval of time that the host must wait for a response from the service processor before assuming that the service processor is not going to respond." Thus, there are no steps between sending the warning and receiving the acknowledgement or timeout, and any communication occurring between these events is strictly assumption.

Looking at the disputed claim language, all that is required is halting executable instruction communications with the co-processor. No period of time for halting communications is claimed, and thus, the fact that in Forsman communication from the service processor to the host processor may exist by way of an acknowledgement message is not outside the bounds of the claim. Forsman explicitly describes wherein the host processor sends a warning message to the service processor and then waits for acknowledgement, or determines a timeout has occurred (column 5, lines 10-22 and figure 3, steps 304-306). In either case, the host processor is waiting, and therefore communications to the service processor are halted.

For at least these reasons, the examiner concludes that Forsman teaches the halt communications module as recited in claim 11.

(11) Related Proceedings Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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12/19/08

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